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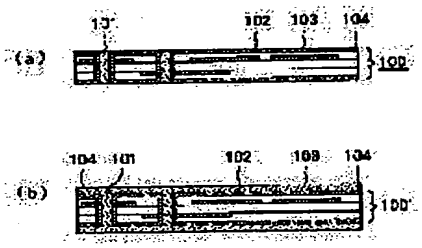
(54) BUILDUP MULTILAYER WIRING BOARD AND MANUFACTURE THEREOF

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a built-up multilayer board, which is equipped with a flat inner layer board and high in reliability and a manufacturing method thereof, wherein a specific hole filling process which elongates a board manufacturing process can be dispensed with, and the inner board can be manufactured by filling many plated through-holes of high aspect ratio with various filling material.

SOLUTION: A frame-like conductor pattern 104 is formed on a base board wiring layer 102 and the periphery of a board, being isolated electrically from the wiring layer 102 and surrounding the wiring layer 102, a solvent-free fluid high-molecular precursor is placed on the frame-like conductor pattern 104, and after a plated through-hole 101 inside and gaps between wirings are evacuated, the precursor is filled into the plated through-hole and the gap and is cured under a hydrostatic pressure, the plated through-hole 101 is filled up, and the inner board is planarized being kept free of defects.



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CLAIMS

[Claim(s)]
[Claim 1] one [at least] penetration plating through hole [which connects both sides electrically], and field top -- level wiring -- the conductor of the shape of a frame formed in the periphery section of a inner layer substrate so that the wiring layer on said inner layer substrate might be electrically independent and said wiring layer might be surrounded in the build up multilayer-interconnection substrate equipped with the inner layer substrate which has the wiring layer which consists of a conductor -- the build up multilayer-interconnection substrate characterized by to be arranged the metal pattern.
[Claim 2] a frame-like conductor -- the wiring layer by which the metal pattern was formed on the same side -- thick -- and -- at least -- a front wiring layer top -- the conductor of the shape of said frame -- the conductor of the shape of said frame regulated in the height of a metal pattern -- the build up multilayer-interconnection substrate according to claim 1 characterized by arranging the layer insulation layer which forms a metal pattern and an abbreviation same flat surface.
[Claim 3] The manufacture approach of the build up multilayer-interconnection substrate which is the manufacture approach of the build up multilayer-interconnection substrate which carries out laminating formation of a layer insulation layer and the wiring layer by turns on a inner layer substrate, and is characterized by carrying out sequential formation of said inner layer substrate at the process of following the (1) - (6).
(1) one [at least] penetration plating through hole [which connects both sides electrically], and field top -- level wiring -- with the wiring layer which consists of a conductor the conductor formed in the periphery section of a substrate in the shape of a frame so that it might be electrically independent of said wiring layer and said wiring layer might be surrounded -- the process which forms the base substrate which has a metal pattern -- (2) The process which installs metal mold with a flat front face in the wiring layer side of a base substrate, and supplies the fluid macromolecule precursor which does not contain a solvent between this base substrate and metal mold, (3) -- the process which exhausts between metal mold and base substrates, and the conductor with which the fluid giant-molecule precursor which is made to move (4) metal mold in the direction of a base substrate, and does not contain a solvent is adjoined on a base substrate at least -- the process with which it is filled up in a gap and a penetration plating through hole -- (5) Process which picks out a inner layer substrate from the process which pours predetermined hydrostatic pressure on the fluid macromolecule precursor which does not contain a solvent, the process which hardens the fluid macromolecule precursor which does not contain a solvent under (6) hydrostatic pressure, and (7) metal mold.
[Claim 4] the process of (1) -- setting -- the same process as formation of a wiring layer -- a conductor -- a metal pattern -- forming -- subsequently -- alternative -- a conductor -- the conductor more than said wiring layer thickness by which carried out plating processing and piling was carried out by plating thickness on the metal pattern -- the manufacture approach of a build up multilayer-interconnection substrate including the process which forms a metal pattern according to claim 3.
[Claim 5] The manufacture approach of the build up multilayer-interconnection substrate according to

claim 3 which prepares the heights of the height more than wiring layer thickness in the part which does not counter with the conductor of a wiring layer as metal mold used below for the process of (2), and front faces other than the heights of a parenthesis fabricate using flat metal mold.

[Claim 6] The manufacture approach of the build up multilayer-interconnection substrate according to claim 3 which supplies the fluid precursor which does not contain a solvent by the shape of a film in the process (2) which installs metal mold with a flat front face in the wiring layer side of a base substrate, and supplies the fluid macromolecule precursor which does not contain a solvent between this base substrate and metal mold.

[Claim 7] It is the manufacture approach of a build up multilayer-interconnection substrate according to claim 3 under a room temperature which applies and supplies by the shape of the shape of film, and a film, without carrying out melting and making it harden in either [at least] the metal mold which carried out the mold-release processing of the fluid precursor which does not contain a solvent in the process (2) which installs metal mold with a flat front face in the wiring layer side of a base substrate, and supplies the fluid macromolecule precursor which does not contain a solvent between this base substrate and metal mold, or a base substrate.

[Claim 8] the process (3) which exhausts between metal mold and base substrates, and the conductor with which the fluid giant-molecule precursor which is made to move metal mold in the direction of a base substrate, and does not contain a solvent is adjoined on a base substrate at least -- the process (4) with which it is filled up in a gap and a penetration plating through hole -- the process (5) which pours predetermined hydrostatic pressure on the fluid giant-molecule precursor which does not contain a solvent -- wiring on a base substrate -- a conductor -- electric -- an independent conductor -- the manufacture approach of the build up multilayer-interconnection substrate according to claim 3 which the at least 1 section and metal mold of a metal pattern are contacted, and stops migration of metal mold.

[Claim 9] the process (3) which exhausts between metal mold and base substrates, and the conductor with which the fluid giant-molecule precursor which is made to move metal mold in the direction of a base substrate, and does not contain a solvent is adjoined on a base substrate at least -- the process (4) with which it is filled up in a gap and a penetration plating through hole -- The manufacture approach of the build up multilayer-interconnection substrate according to claim 5 which the at least 1 section of the heights of a base substrate and metal mold is contacted, and stops migration of metal mold according to the process (5) which pours predetermined hydrostatic pressure on the fluid giant-molecule precursor which does not contain a solvent.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a build up multilayer-interconnection substrate and its manufacture approach, and relates to the suitable build up multilayer-interconnection substrate for a high-density multilayer-interconnection substrate, a multi chip module substrate, etc. which are especially used for public welfare devices, such as computers, such as a mainframe, a workstation, a personal computer, and a multimedia computer, an ATM switching system for a communication link, and a cellular phone, a video camera, etc., and its manufacture approach.
[0002]
[Description of the Prior Art] Various kinds of things are proposed by the build up substrate which is becoming indispensable to high-performance-izing of electronic equipment, and small-and-light-izing. For example, in order to take the flow of the front flesh side shown in drawing 9 so that it may be indicated by JP,4-148590,A etc., there was a through hole 901 which carried out drilling, and improvement in a wiring consistency and the degree of freedom of a wiring design had a limit. Therefore, recently, the stopgap build up substrate which avoids such a problem by carrying out the laminating of the build up layer 1003 is becoming in use, without losing a wiring field on the substrate with which such a through hole was buried with resin, the conductive paste 1001, etc., as shown in drawing 10 .
[0003] As the approach of stopgap, as the collection of "public presentation [in collaboration] study group build up patchboard and detailed printing technical" lecture summaries, 17-22, 38-51 pages (1997), JP,5-67874,A, etc. have a publication, the ink of dedication was filled up with screen-stencil in the hole, and it has hardened by ultraviolet rays or heat treatment. Moreover, since the size of a hole is called inner layer substrate of a build up substrate, its place which the path called 0.3mm and die length (namely, substrate thickness) called 0.6mm is common.
[0004] There were the following troubles in such a Prior art. The 1st problem is the point that a production process becomes long further compared with the part and the conventional build up substrate which need to grind and turn up flattening of the uneven configuration of each class generated for the outermost wiring layer of a inner layer substrate for multilayering of a build up layer, and need a stopgap process.
[0005] Since a fluidity (restoration nature) and light transmission nature are required for stopgap ink, it is that an ingredient is limited, therefore a limitation is generated also in physical properties, such as thermal resistance and chemical resistance, or ink after hardening, and the 2nd problem has been the failure of application to the severe high performance substrate of process conditions.
[0006] Moreover, as for the 3rd problem, a ******** is mentioned for a stopgap process. This is because the process which grinds a substrate front face and is made flat is required, in order for ink to remain and to form wiring of the removal and following layer on the property of screen-stencil, and on the outskirts of a restoration hole. Furthermore, the 4th problem has a limitation also in the aspect ratio of the hole which can be filled up also with exclusive ink, and the number of holes per unit area with which it can be filled up actually.
[0007] then, the conductor with which the fluid giant-molecule precursor which this invention person etc. makes move metal mold in the direction of a base substrate as indicated to JP,6-334343,A, and does not contain a solvent in order to solve these troubles is adjoined on a base substrate at least -- the manufacture approach with which it is filled up in a gap and a penetration plating through hole was proposed.
[0008]
[Problem(s) to be Solved by the Invention] thus, there is no void, as compared with other conventional techniques, is boiled markedly and is excellent in the point that a metal mold side is imprinted and a substrate front face is also referred to as flat at the insulating layer the formed outermost wiring top and in a through hole. However, in the high density multilayer substrate, since the base substrate was thin, a substrate tended to curve, and the new problem which says that it faces attaining multilayering

by the built-up method by making this into a inner layer substrate, and dependability falls occurred. moreover -- structural -- the wiring substrate of high density -- setting -- the outermost wiring layer of a inner layer substrate -- electromagnetism -- it is important to carry out a seal and consideration according to rank was not carried out about this.

[0009] Therefore, it is in the purpose of this invention canceling the above-mentioned conventional trouble. The 1st purposes surround the periphery section of a inner layer substrate with a frame-like conductor pattern so that the outermost wiring layer of a inner layer substrate may be surrounded. It is in realizing a reliable built-up multilayer substrate by carrying out electromagnetic shielding of the circuit formed on the same flat surface. Even if the 2nd purpose uses a thin base substrate, it is to realize the manufacture approach of the improved built-up multilayer substrate which can be multilayered by the built-up method, without reducing dependability.

[0010]

[Means for Solving the Problem] In the build up multilayer-interconnection substrate equipped with the inner layer substrate which has the wiring layer which consists of a conductor one [at least] penetration plating through hole [where the 1st purpose of the above connects both sides electrically], and field top -- level wiring -- the conductor of the shape of a frame formed in the periphery section of a inner layer substrate so that it might be electrically independent of the wiring layer on said inner layer substrate and said wiring layer might be surrounded -- it is attained by the build up multilayer-interconnection substrate characterized by arranging the metal pattern.

[0011] and -- desirable -- a frame-like conductor -- the wiring layer formed on the same side in the metal pattern -- thick -- carrying out -- and -- at least -- a front wiring layer top -- the conductor of the shape of said frame -- it regulates in the height of a metal pattern -- having -- the conductor of the shape of said frame -- it is considering as the configuration in which the layer insulation layer which forms a metal pattern and an abbreviation same flat surface was arranged.

[0012] Moreover, the 2nd purpose of the above is attained by the manufacture approach of the build up multilayer-interconnection substrate which is the manufacture approach of the build up multilayer-interconnection substrate which carries out laminating formation of a layer insulation layer and the wiring layer by turns on a inner layer substrate, and is characterized by carrying out sequential formation of said inner layer substrate at the process of following the (1) - (6).

[0013] (1) one [at least] penetration plating through hole [which connects both sides electrically], and field top -- level wiring -- with the wiring layer which consists of a conductor the conductor formed in the periphery section of a substrate in the shape of a frame so that it might be electrically independent of said wiring layer and said wiring layer might be surrounded -- the process which forms the base substrate which has a metal pattern -- (2) The process which installs metal mold with a flat front face in the wiring layer side of a base substrate, and supplies the fluid macromolecule precursor which does not contain a solvent between this base substrate and metal mold, (3) -- the process which exhausts between metal mold and base substrates, and the conductor with which the fluid giant-molecule precursor which is made to move (4) metal mold in the direction of a base substrate, and does not contain a solvent is adjoined on a base substrate at least -- the process with which it is filled up in a gap and a penetration plating through hole -- (5) Process which picks out a inner layer substrate from the process which pours predetermined hydrostatic pressure on the fluid macromolecule precursor which does not contain a solvent, the process which hardens the fluid macromolecule precursor which does not contain a solvent under (6) hydrostatic pressure, and (7) metal mold.

[0014] And it sets at the process of (1) preferably. Plating processing is carried out on a metal pattern. the same process as formation of a wiring layer -- a conductor -- a metal pattern -- forming -- subsequently -- alternative -- a conductor -- the conductor more than said wiring layer thickness by which piling was carried out by plating thickness -- as metal mold used below for the process of (2), including the process which forms a metal pattern The conductor of a wiring layer is that prepare the heights of the height more than wiring layer thickness in the part which does not counter, and front

faces other than the heights of a parenthesis fabricate using flat metal mold.
[0015]
[Embodiment of the Invention] The configuration of the eight-layer wiring substrate which carried out the laminating of the build up layer of every front rear-face two-layer on the four-layer wiring substrate which has the penetration plating through hole made up for hereafter, and the gestalt of operation of the manufacture approach are explained.
[0016] That is, the inner layer substrate 100 which carries out the laminating of the build up layer, and the cross-section structure of 100' are shown in drawing 1 (a) and drawing 1 R> 1 (b). It considered as the wiring substrate which serves as the conductor pattern 104 of the shape of a frame formed in the periphery of a substrate from an insulating layer 103 so that the penetration plating through hole 101 filled up with the insulating material, the outermost wiring layer 102, and the outermost wiring layer might be surrounded, and the insulating material and the outermost insulating layer 103 of a substrate with which it fills up in a penetration plating through hole were formed with the same ingredient, and it considered as structure with a flat substrate front face.
[0017] The diameter of the penetration plating through hole 101 filled up with the insulating material from the range of 1-1000 micrometers Die length (namely, inner layer substrate thickness) is selectable from the range of 0.05-5mm to arbitration. Moreover, the surface smoothness on the front face of a substrate the case of the structure of drawing 1 (a) -- the frame-like conductor pattern 104 and the conductor of the outermost wiring layer 102 -- the thickness of a conductor layer less than 10% [the difference of the thickness of the outermost insulating layer 103 which filled the gap, and the thickness of these conductor layers] or the case of the structure of drawing 1 (b) -- the frame-like conductor pattern 104 and the conductor of the outermost wiring layer 102 -- a gap is filled and the thickness variation of the wrap insulating layer 103 is less than 10% of insulating thickness about these conductor layers.
[0018] What is necessary is just to form a wiring layer and an insulating layer by turns with a well-known lamination technique on the inner layer substrate of drawing 1 R> 1, in order to manufacture a build up multilayer substrate. As shown in drawing 1 (b), in the case of the structure covered by the outermost insulating layer 103, the frame-like conductor pattern 104 and outermost wiring layer 102 top The electrical installation with the build up layer of the following layer to 105 in a hole which carried out laser beam machining until the conductor 102 was exposed to the outermost insulator layer 103 as shown in drawing 2 What is necessary is just to carry out by forming the wiring conductor pattern of the 5th layer and the 6th layer with the restoration plating by the conventional build up substrate method 301 as shown in drawing 3 by the galvanizing method, or nonelectrolytic plating 401 like drawing 4 . The diameter of such a hole 105 can be processed by 1-50 micrometers which cannot be formed with the photosensitive interlayer insulation film ingredient for build up substrates, and it is desirable for the bore diameter on the front face of an insulating layer to be more than a diameter of exposure of a conductor (taper configuration).
[0019] Moreover, as a laser kind at the time of breaking a hole in an insulator layer by laser beam machining, low cost YAG or carbonic acid laser is desirable. Before forming wiring in 105 in a hole which carried out [above-mentioned] laser beam machining, clarification, surface roughening, and the connection dependability of wiring that will be formed if hydrophilization is carried out not only improve, but the yield [wiring / wiring in a hole like drawing 3 and / of a inner layer substrate front face] of coincidence formation improves the substrate front face 503 containing a hole wall and a pars basilaris ossis occipitalis by oxidizing quality liquid processing or dry washing processing.
[0020] As such an oxidizing quality liquid, although the mixed acid of an alkaline potassium permanganate water solution or concentrated sulfuric acid, and a chromic acid is desirable, an alkaline potassium permanganate water solution is more desirable from an environmental side. Moreover, as dry washing processing, it is desirable that they are oxygen plasma ashing, UV/ozonization, or at least one approach in corona discharge.

[0021] Furthermore, if the aspect ratio of this laser hole becomes large, as shown in drawing 5 , it was completely filled up with the inside of a hole upwards, and the restoration section 501 can be evenly made into the same field as the inner layer substrate front wiring section 502, so that it may be indicated by JP,8-78846,A, for example.
[0022] Although the front wiring section 502 shown in drawing 5 serves as a wiring conductor pattern of the 5th layer and the 6th layer, it can carry out the laminating of the pattern of the 7th layer and the 8th layer by repeating the formation process of a well-known insulating layer and a conductor layer after this.
[0023] Next, the formation process of the inner layer substrate for build up substrates shown by drawing 1 is explained using process drawing of drawing 6 . However, although the base substrate 603 for forming the inner layer substrate 100 forms four-layer wiring, it omits the inner layer section here and has displayed only the outermost layer.
[0024] (1) the penetration plating through hole 601 which connects both sides electrically first as shown in drawing 6 (a) -- having -- one [at least] field top -- level wiring -- the conductor formed in the periphery section of a substrate in the shape of a frame so that the wiring layer 102 which consists of a conductor, and this wiring layer might be electrically independent and a wiring layer might be surrounded -- form the base substrate 603 which has the metal pattern 104. in addition, a conductor -- although the metal pattern 104 is formed at the same pattern formation process as a wiring layer 102, it may form a wiring layer 102 with the conductor of the different quality of the material according to another process.
[0025] (2) As shown in drawing 6 (b), install the metal mold 604 with a flat front face in the wiring layer side of the base substrate 603, and supply the fluid macromolecule precursor (raw material resin which forms an insulating layer) 605 which does not contain a solvent between this base substrate and metal mold. In addition, 607 is packing which consists of an elastic body which closes the upper and lower sides of metal mold, and is using packing made of silicone rubber here.
[0026] (3) As shown in drawing 6 (b) -> drawing 6 (c), exhaust between metal mold 604 and the base substrates 603 from an exhaust port 606.
[0027] (4) the conductor with which the fluid giant-molecule precursor 605 which is made to move metal mold in the direction of a base substrate, and does not contain a solvent as shown in drawing 6 (c) -> (d) is adjoined on a base substrate at least -- it is filled up in a gap and a penetration plating through hole. In order to make restoration easy, the temperature up of the metal mold is carried out to predetermined temperature, and the fluidity of the macromolecule precursor 605 is raised. the conductor with which the movement magnitude of metal mold was formed in the periphery section of a wiring layer 102 and a substrate in the shape of a frame -- it carries out until the flat surface of metal mold contacts the front face of the metal pattern 104.
[0028] (5) As shown in drawing 6 (d), from the addition opening 606, pour inert gas, such as nitrogen and air, into the fluid macromolecule precursor 605 which does not contain a solvent, and pour predetermined hydrostatic pressure on it.
[0029] (6) Drawing 6 (d) As shown in -> (e), the fluid macromolecule precursor which does not contain a solvent is hardened and mold omission is made the bottom of hydrostatic pressure.
[0030] the conductor formed in a wiring layer 102 and the substrate periphery section in the shape of a frame of the above process -- while filling up between the ****** wiring layers 102 and the gap of a wiring layer 102 and a conductor pattern 104 with an insulating layer 102, exposing the front face of the metal pattern 104, the inner layer substrate 100 which has the through hole 101 where the inside of a through hole 601 was also filled up into coincidence with the insulating layer 102 is obtained.
[0031] moreover, the conductor pattern 104 (wiring layer 102 is electrically independent) top formed in ** shown in drawing 7 R> 7 (a) in the shape of a frame as a modification of the above-mentioned process (1) at the substrate periphery section -- a conductor -- plating -- carrying out -- the conductor of the height more than wiring layer thickness -- the metal pattern 702 is formed. this

conductor -- in the height of the metal pattern 702, the thickness of the insulating layer 103 by which a laminating is carried out after that on a wiring layer 102 is regulated.

[0032] after the above-mentioned process (3), (4), and (5) and this conductor, if the fluid macromolecule precursor which the at least 1 section of the metal pattern 702 and the flat surface of metal mold are contacted, and does not include migration of metal mold for a solvent under a stop and hydrostatic pressure is hardened As shown in drawing 7 R> 7 (b), while forming the build up insulating layer 705 on the outermost wiring layer 102 of the base substrate 703, stopgap 706 of the penetration plating through hole 601 is also made to coincidence.

[0033] a conductor -- although there is no limit in the formation location of the metal pattern 702, in order to control insulating thickness with high precision, at least, on the conductor pattern 104 of the base substrate periphery section, it is required, and should prepare also in the wiring field periphery section desirably.

[0034] Thus, a metal mold side is imprinted also for a front face by there being nothing by the insulating layer the formed outermost wiring layer top and in a through hole, and the void is flat to it so that it may indicate to JP,6-334343,A which this invention person etc. proposed previously. Furthermore, by this manufacture approach, operation of the process after (4) is possible under heating, the fluid macromolecule precursor which does not contain a solid solvent without a fluidity also carries out heating fusion, is made to hypoviscosity-ize at a room temperature, use becomes possible, and the width of face of ingredient selection spreads. Therefore, even if a viscosity rise will be caused, the filler content in an ingredient can be adjusted, a coefficient of thermal expansion can be doubled with a base substrate, and the depression of the stopgap section and a swelling can be controlled.

[0035] Furthermore, after exhausting the inside of a through hole, since a gap is filled, application of the base substrate which has the high penetration plating through hole of an aspect ratio with a thick base substrate or sheet metal in a minor diameter is also possible. moreover -- actual -- a conductor -- the insulator layer which remains among these since metal mold moves until it touches the metal pattern 702 mostly -- about several micrometers -- the amount -- a conductor -- the formation precision of the metal pattern 702 -- depending -- a little low conductor -- the film only remains in the metal pattern section. therefore, the outermost insulator layer thickness 705 -- a conductor -- the thickness of the metal pattern 702 -- controllable -- such a conductor -- the galvanizing method is common, as the formation approach of a metal pattern, when a higher precision is required, the method of nonelectrolytic plating is desirable, and formation time amount is thought as important rather -- electroplating is good if it becomes. since the conductor pattern 104 of the shape of a frame used as the substrate of performing such plating is formed in coincidence in case a wiring layer is formed as shown in drawing 7 , the amount of plating is shortened -- having -- a conductor -- the formation precision of a metal pattern is raised and formation time amount can be shortened.

[0036] the case where an insulating layer is formed on the outermost wiring layer as mentioned above -- wiring -- a conductor -- electric -- the conductor of the height more than independent wiring layer thickness, conversely, as shown in drawing 8 , the heights 801 for insulating thickness control may be formed in a change of the metal pattern 702 at metal mold 606. By the conductor of a wiring layer, and the part by which it does not counter, at least, such heights are also required for the base substrate periphery section, and it is desirable that it is also in the wiring field periphery section. The formation may cut a metal mold front face by the suitable machining method, and even if it carries out by etching following plating or it, it is not cared about. Moreover, that to which adhesion, welding, etc. used the member for the convex configurations of an exact dimension as metal mold can also be used.

[0037] Although the fluid macromolecule precursor which does not contain a solvent is used as resin which constitutes the insulating layer of a inner layer substrate in this invention, this is because he wants to control generating of gas in case between wiring layers and a through hole are filled up with resin using metal mold. It is because gas will occur at the time of restoration, a void will occur in an insulating layer and an insulating property will be remarkably degraded, if a solvent is included. The fluid

macromolecule precursor which does not contain a solvent is thermosetting resin and thermoplastics containing the filler the object for coefficient-of-thermal-expansion adjustment, and for roughening **** formation, and has a liquefied thing and a solid thing. When these are liquefied, what is necessary is just to use it as the shape of liquid membrane applied to either [at least] the metal mold which carried out mold release processing, or a base substrate, and, in a solid case, it can be used as the shape of a film, and the shape of a film which fixed without carrying out melting to either [at least] the metal mold which carried out mold release processing, or a base substrate, and making it harden.

[0038]

[Example] An example explains concretely the configuration and the manufacture approach of an eight-layer wiring substrate which carried out the laminating of the build up layer of every front rear-face two-layer on the four-layer wiring substrate which has hereafter the penetration plating through hole made up for in this invention.

[0039] <Example 1> The manufacture approach of the eight-layer wiring substrate of the structure shown in drawing 11 is shown below. A production process follows process drawing shown in drawing 6 . First, the base substrate (it corresponds to 603 of drawing 6 (a)) applicable to the layer of the center section of drawing 11 is manufactured. On both sides of the prepreg (glass epoxy group plate) of 0.1mm thickness, it put two 18-micrometer thickness copper foil at a time on both sides of the substrate which etched 500mm angle and 35-micrometer thickness copper foil of the double-sided copper clad laminate of 1.6mm of board thickness which made copper foil rival into both sides of a glass epoxy group plate (laminate which sank the epoxy resin into the glass fiber), and formed the 4th wiring layer 1104 and the 5th wiring layer 1105 in them, and laminating adhesion was carried out.

[0040] After carrying out 35000 through hole dawn processing to the produced double-sided plate with the drill of 0.2mm diameter, carrying out panel plating, etching double-sided copper foil and forming a circuit pattern, the base substrate in which the conductor pattern 104 (wiring layers 1103 and 1106 are electrically independent) formed in the penetration plating through hole 1109, the 3rd wiring layer 1103, the 6th wiring layer 1106, and the substrate periphery section in the shape of a frame was formed was produced. This corresponds to the drawing 6 (a) process.

[0041] The following processes are performed according to the procedure explained by drawing 6 (b) - drawing 6 (e). Melting of the constituent of the biphenyl system epoxy resin which did 50 volume % mixing of the silica filler of 2 micrometers of mean diameters, and phenol resin was carried out at 80 degrees C, and the front face which applied the fluorine system heatproof release agent passed and carried out air cooling on flat plate-like metal mold, and carried out melting fixing at the shape of a film.

[0042] The base substrate produced previously was pinched between these two metal mold, between metal mold was exhausted to 10Torr(s), metal mold was heated at 70 degrees C, melting of the epoxy constituent was carried out, and it was filled up between the 3rd and 6th wiring and in the penetration plating through hole. And pneumatic pressure 0.8MPa is added between compression-pressure 0.9MPa which sandwiches a stop and metal mold for exhaust air, and metal mold. Metal mold is moved to the 3rd and 6th wiring layer, and the bottom of hydrostatic pressure and metal mold are heated. At 160 degrees C For 30 minutes, 180 degrees C -- for 60 minutes and an epoxy constituent -- hardening -- the outermost wiring layer -- a conductor -- the penetration plating through hole produced the inner layer substrate 1110 of flat four-layer wiring for build up substrates filled up with the same defect-free insulating material between.

[0043] The above-mentioned inner layer substrate 1110 Subsequently, the inside of a potassium permanganate-sodium-hydroxide water solution, A top is defecated and a commercial photosensitive layer insulation ingredient is used as a layer insulation layer. 80 degrees C -- for 45 minutes, the inside of 3% hydroxylamine sulfate water solution, and 23 degrees C -- for 5 minutes -- processing -- the 3rd and 6th wiring layer -- a conductor -- by the formation approach of a well-known laminating pattern The build up laminated circuit board of eight layers of wiring totals was manufactured without having carried out the laminating of the build up layer 1111 containing the 1st wiring layer 1101 and the 2nd

wiring layer 1102, and grinding it.
[0044] Without camber occurring, when carrying out the laminating of the build up layer 1111 since the frame-like conductor pattern 104 is formed in the periphery section of the inner layer substrate 1110, since this build up laminated circuit board had the effectiveness that the frame-like conductor pattern 104 moreover carries out electromagnetic shielding of the wiring layer of that contrant region, it has realized the reliable high density multilayer-interconnection substrate. Moreover, in case the conductor pattern 104 of the shape of a frame formed in the substrate periphery section manufactures a inner layer substrate under hydrostatic pressure with metal mold, it also has the operation effectiveness of packing.
[0045] <Example 2> The manufacture approach of the eight-layer wiring substrate of the structure shown in drawing 12 is shown below. At the time of formation of the 3rd wiring layer 1203 and the 6th wiring layer 1206, in case a base substrate is produced like an example 1, these wiring layers leave the frame pattern 1209 which became independent electrically, and form the plating copper 1210 of 50**2-micrometer thickness only in this part by electroplating further so that a substrate periphery may be surrounded by 10mm width of face. and the example 1 -- the same -- carrying out -- an epoxy system insulating layer -- forming -- the outermost wiring layer top and a conductor -- the inner layer substrate 1212 of four-layer wiring for build up substrates which already carried out 1 stratification of the flat build up insulating layer 1211 (52**1-micrometer thickness) with which between and a penetration plating through hole were covered and filled up with the same defect-free insulating material was produced.
[0046] Subsequently, the cylindrical hole with 50 micrometers [of diameters of upper] and a diameter of bottom of 40 micrometers was broken with carbon-dioxide-gas-laser equipment in the position of the build up insulating layer 1211 on the 3rd and 6th wiring layer, and after processing this inner layer substrate for 5 minutes at 23 degrees C for 40 minutes and among 3% hydroxylamine sulfate water solution by 80 degrees C among the potassium permanganate-sodium-hydroxide water solution, the nonelectrolytic plating copper film of 1-micrometer thickness was formed in both sides. The dry film resist which carried out hole dawn processing to the position containing a laser hole was formed, the conductor pattern of the 2nd wiring layer 1202 and the 7th wiring layer 1207 was formed by electroplating, and etching removal of the parts other than exfoliation and wiring of a nonelectrolytic plating copper film was carried out for the dry film. Furthermore, the one-layer laminating was carried out using the commercial layer insulation ingredient for laser beam machining, the build up layer 1213 was formed, and the build up substrate of eight layers of wiring totals was manufactured.
[0047] Although the ****** pattern 1209 of the substrate periphery section formed at the same process as the outermost wiring layer of the inner layer substrate 1212 has the same effectiveness as an example 1, it has the effectiveness that the thickness of the flat build up insulating layer 1211 is correctly controllable, by controlling the thickness of the plating copper pattern 1210 further formed on it in this example.
[0048] <Example 3> The manufacture approach of the eight-layer wiring substrate of the structure shown in drawing 13 is shown below. The base substrate was produced like the example 1. The metal mold made from stainless steel with the flat front face which carried out [the front face] grinding polish and was produced so that it might remain in the height whose part which counters the location 1309 which encloses the periphery section, the 3rd wiring layer 1303, and the 6th wiring layer 1306 of a base substrate in the shape of a frame by 10mm width of face is 100 micrometers is used. Like an example 2 the outermost wiring layer top and a conductor -- the inner layer substrate 1311 of four-layer wiring for build up substrates which already carried out 1 stratification of the flat build up insulating layer 1310 with which between and a penetration plating through hole were covered and filled up with the same defect-free insulating material was produced.
[0049] Still like the example 2, the cylindrical hole with 30 micrometers [of diameters of upper] and a diameter of bottom of 25 micrometers was broken with YAG laser equipment in the position of the build

up insulating layer 1310 on the 3rd and 6th wiring layer, this inner layer substrate was processed in the hydroxylamine sulfate water solution a potassium permanganate-sodium-hydroxide water solution / 3%, oxygen plasma-asher processing was carried out further, and the nonelectrolytic plating copper film of 1-micrometer thickness was formed in both sides. The dry film resist which carried out hole dawn processing to the position containing a laser hole was formed, and electroplating was completely filled up with 1312 in a laser hole, and also the conductor pattern of the 2nd flat wiring layer 1302 and the 7th wiring layer 1307 was formed, and etching removal of the parts other than exfoliation and wiring of a nonelectrolytic plating copper film was carried out for the dry film. Furthermore, the one-layer laminating was carried out using the commercial layer insulation ingredient for laser beam machining, the build up layer 1313 was formed, and the build up substrate of eight layers of wiring totals was manufactured.

[0050] The effectiveness of the conductor pattern 104 of the shape of a frame prepared in the periphery section of the inner layer substrate 1311 was acquired like the case of an example 1. In this example, since the periphery of the build up insulating layer 1310 approached inside and has exposed the periphery section 1309 of a base substrate further, the periphery section of a conductor pattern 104 and the build up insulating layer 1310 can be protected, and dependability is raised further.

[0051] <Example 4> In the example 1, the epoxy constituent which forms an insulating layer was replaced with the constituent of the bisphenol A system epoxy resin which did 50 volume % mixing of the silica filler of 1.5 micrometers of mean diameters, and a dicyandiamide, and this was applied and supplied at the room temperature on the metal mold which counters a base substrate top face and an inferior surface of tongue. And after exhausting between metal mold for 5 minutes at a room temperature, it was operated similarly, and the build up substrate of the structure shown in drawing 11 was manufactured.

[0052] <Example 5> In the example 2, the epoxy constituent which forms an insulating layer was replaced with the constituent of the bisphenol A system epoxy resin which did 50 volume % mixing of the silica filler of 1.5 micrometers of mean diameters, and a dicyandiamide, and this was applied and supplied at the room temperature on the metal mold which counters a base substrate top face and an inferior surface of tongue. The base substrate used the thing of 4.0mm of board thickness, operated it like the example 4, and the build up substrate of the structure shown in drawing 12 was manufactured. In addition, the potassium permanganate-sodium-hydroxide processing time was carried out in 30 minutes.

[0053] <Example 6> In the example 3, the epoxy constituent which forms an insulating layer was replaced with the constituent of the bisphenol A system epoxy resin which did 50 volume % mixing of the silica filler of 1.5 micrometers of mean diameters, and a dicyandiamide, and this was applied and supplied at the room temperature on the metal mold which counters a base substrate top face and an inferior surface of tongue. The base substrate was 0.3mm of board thickness, it used the thing which was produced by carbon dioxide gas laser and which was finished and prepared the penetration plating through hole of 30 micrometers of diameters, operated it like the example 4, and manufactured the build up substrate of the structure shown in drawing 13 . In addition, the potassium permanganate-sodium-hydroxide processing time was carried out in 30 minutes.

[0054] <Example 7>. In the example 5, the epoxy constituent which forms an insulating layer was replaced with the liquefied BT resin (bismaleimide-triazine resin: Mitsubishi Gas Chemical make) which did 40 volume % mixing of the silica filler of 1.5 micrometers of mean diameters, and the build up substrate of the structure shown in drawing 12 was manufactured. Hardening conditions carried out 30 minutes, and 60 minutes and the 160-degree-C potassium permanganate [220 degree-C]-sodium-hydroxide processing time in 20 minutes.

[0055]

[Effect of the Invention] As mentioned above, this invention was able to attain the desired end. That is, the periphery section of a inner layer substrate was able to be surrounded with the frame-like conductor pattern so that the outermost wiring layer of a inner layer substrate might be surrounded, and the reliable built-up multilayer substrate was able to be realized by carrying out electromagnetic shielding of the circuit formed on the same flat surface.

[0056] Moreover, even if it used the thin inner layer substrate, the manufacture approach of the improved built-up multilayer substrate which can be multilayered by the built-up method, without reducing dependability was realizable.

[0057] The penetration plating through hole into which the inner layer substrate for carrying out the laminating of the build up layer was specifically filled up with the insulating material, By constituting from an insulating layer which embedded at least the gap of between the outermost wiring layers and the outermost wiring layer, and the conductor pattern of the shape of a frame prepared in the substrate periphery by the same insulating material, and making a substrate front face into flat structure a frame-like conductor pattern prevents the curvature of a substrate and it has the effectiveness which carries out magnetic shielding of the wiring layer formed in the same flat surface, and the dependability and the yield of a build up multilayer substrate were able to be boiled markedly, and were able to be raised.

[0058] after forming a frame-like conductor pattern in the periphery section of a inner layer substrate independently electrically with the wiring layer of the outermost layer of a inner layer substrate -- further -- this conductor pattern top -- the 2nd conductor of the height more than wiring layer thickness -- if the metal pattern is prepared -- the outermost wiring layer top -- these conductors -- stopgap of a penetration plating through hole can be performed at the same time it forms the flat insulating layer by which thickness control was carried out by metal patterns.

[0059] Moreover, since operation under heating is possible for this process, where it carried out melting also of the hyperviscosity stopgap ingredient inferior to a fluidity if needed and viscosity is lowered, it can be used. Therefore, although viscosity goes up in order to lower a coefficient of thermal expansion, in order to increase a filler content, to become possible to optimize an ingredient configuration and to correspond, and for polish etc. to be able to form the front face of a inner layer substrate without a special process evenly and to carry out the laminating of the build up layer to coincidence, required thermal resistance and chemical resistance can also be given on a process. Furthermore, at this process, since a stopgap ingredient is made to flow and it is filled up after exhausting the inside of a penetration plating through hole, there is no defect of restoration and the effect of the number of holes per unit area does not once receive it in essence, either.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The sectional view showing an example of the structure of the inner layer substrate for build up substrates concerning this invention.

[Drawing 2] The sectional view showing an example of the structure of the inner layer substrate for build up substrates concerning this invention.

[Drawing 3] The sectional view showing an example of the electrical installation gestalt of the inner layer

substrate for build up substrates and build up layer concerning this invention.
[Drawing 4] The sectional view showing an example of the electrical installation gestalt of the inner layer substrate for build up substrates and build up layer concerning this invention.
[Drawing 5] The sectional view showing an example of the electrical installation gestalt of the inner layer substrate for build up substrates and build up layer concerning this invention.
[Drawing 6] Process drawing showing an example of the manufacture approach of the inner layer substrate for build up substrates concerning this invention.
[Drawing 7] Process drawing showing an example of the manufacture approach of the inner layer substrate for build up substrates concerning this invention.
[Drawing 8] Process drawing showing an example of the manufacture approach of the inner layer substrate for build up substrates concerning this invention.
[Drawing 9] The sectional view showing an example of the structure of the conventional build up substrate.
[Drawing 10] The sectional view showing an example of the structure of the conventional build up substrate.
[Drawing 11] The sectional view showing an example of the structure of the build up substrate concerning this invention.
[Drawing 12] The sectional view showing an example of the structure of the build up substrate concerning this invention.
[Drawing 13] The sectional view showing an example of the structure of the build up substrate concerning this invention.
[Description of Notations]
100,100' -- Inner layer substrate,
101 -- Penetration plating through hole,
102 -- Wiring layer,
103 -- Insulating layer,
104 -- Frame-like conductor pattern,
105 -- The interior of a laser-beam-machining hole,
301 -- wiring for the upper connection formed by the conventional build up substrate method -- a conductor,
wiring for the upper connection formed with 401 -- nonelectrolytic plating -- a conductor,
501 -- wiring -- the laser hole upper part filled up with the conductor,
502 -- Inner layer substrate surface wiring layer,
503 -- Inner layer substrate front face,
601 -- Penetration plating through hole,
603 -- Base substrate,
604 -- Metal mold,
605 -- Fluid macromolecule precursor which does not contain a solvent,
606 -- An exhaust port, hydrostatic-pressure addition opening,
607 -- Packing,
702 -- a conductor -- a metal pattern,
705 -- Build up insulating layer,
706 -- The stopgap section of a penetration plating through hole,
801 -- Heights for insulating thickness control,
901 -- Penetration plating through hole,
902 -- Inner layer substrate for build up substrates,
903 -- Build up layer,
1001 -- Stopgap resin, conductive paste,
1002 -- Inner layer substrate for build up substrates,

1003 -- Build up layer,
1101, 1201, 1301 -- The 1st wiring layer,
1102, 1202, 1302 -- The 2nd wiring layer,
1103, 1203, 1303 -- The 3rd wiring layer,
1104, 1204, 1304 -- The 4th wiring layer,
1105, 1205, 1305 -- The 5th wiring layer,
1106, 1206, 1306 -- The 6th wiring layer,
1207 1307 -- The 7th wiring layer,
1208 1308 -- The 8th wiring layer
1109 -- Penetration plating through hole,
1110 -- Inner layer substrate for build up substrates,
1111 -- Build up layer,
1209 -- Frame pattern,
1210 -- Plating copper,
1211 -- Build up insulating layer,
1212 -- Inner layer substrate for build up substrates,
1213 -- Build up layer,
1309 -- Base substrate periphery section,
1310 -- Build up insulating layer,
1311 -- Inner layer substrate for build up substrates,
1312 -- The interior of a laser hole,
1313 -- Build up layer.

[Translation done.]

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最終頁に続く

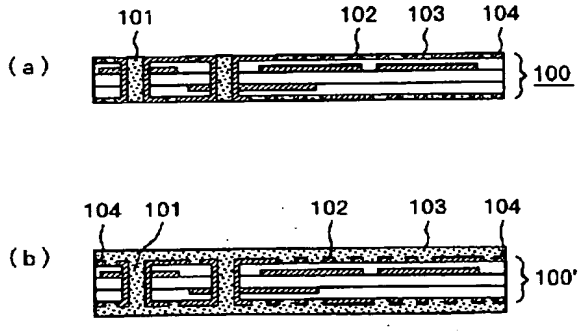
(54)【発明の名称】　ビルドアップ多層配線基板及びその製造方法

(57)【要約】

【課題】ビルドアップ基板製造工程が長くなるような特別な穴埋め工程を必要とせず、広範な穴埋め材料で、高アスペクト比な多数の貫通めっきスルーホールを充填して製造が可能な表面が平坦な内層基板を備えた高信頼性のビルドアップ多層基板とその製造方法を実現する。

【解決手段】ベース基板の配線層上、及び基板周縁部に配線層とは電気的に独立して配線層を取り囲むように形成された額縁状の導体パターン上に無溶剤の流動性高分子前駆体を置き、貫通めっきスルーホール内、配線間隙を排気した後、前駆体を充填し、静水圧をかけながら硬化して、欠陥無く、貫通めっきスルーホールの穴埋めと、内層基板の平坦化とを行う。

図　1



１００，１００'…内層基板　１０１…貫通めっきスルーホール
１０２…配線層　１０３…絶縁層　１０４…額縁状導体パターン

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【特許請求の範囲】

【請求項１】両面を電気的に接続する貫通めっきスルーホールと、少なくとも一方の面上に水平配線導体からなる配線層とを有する内層基板を備えたビルドアップ多層配線基板において、前記内層基板上の配線層とは電気的に独立で、前記配線層を取り囲むように内層基板の周縁部に形成された額縁状の導体金属パターンが配設されていることを特徴とするビルドアップ多層配線基板。

【請求項２】額縁状の導体金属パターンは、同一面上に形成された配線層よりも厚く、かつ少なくとも前配線層上には、前記額縁状の導体金属パターンの高さで規制された前記額縁状の導体金属パターンと略同一平面を形成する層間絶縁層が配設されていることを特徴とする請求項１記載のビルドアップ多層配線基板。

【請求項３】内層基板上に層間絶縁層と配線層とを交互に積層形成するビルドアップ多層配線基板の製造方法であって、前記内層基板を下記（１）～（６）の工程で順次形成することを特徴とするビルドアップ多層配線基板の製造方法。

（１）両面を電気的に接続する貫通めっきスルーホールと、少なくとも一方の面上に水平配線導体からなる配線層と、前記配線層とは電気的に独立で前記配線層を取り囲むように基板の周縁部に額縁状に形成された導体金属パターンとを有するベース基板を形成する工程、（２）ベース基板の配線層側に表面の平坦な金型を設置し、このベース基板と金型との間に溶剤を含まない流動性高分子前駆体を供給する工程、（３）金型とベース基板との間を排気する工程、（４）金型をベース基板方向へ移動させて溶剤を含まない流動性高分子前駆体をベース基板上の少なくとも隣接する導体間隙と貫通めっきスルーホール内に充填する工程、（５）溶剤を含まない流動性高分子前駆体に所定の静水圧をかける工程、（６）静水圧下において溶剤を含まない流動性高分子前駆体を硬化する工程及び（７）金型から内層基板を取り出す工程。

【請求項４】（１）の工程においては、配線層の形成と同一工程で導体金属パターンを形成し、次いで選択的に導体金属パターン上にめっき処理し、めっき厚さ分だけかさ上げされた前記配線層厚以上の導体金属パターンを形成する工程を含む請求項３記載のビルドアップ多層配線基板の製造方法。

【請求項５】（２）の工程以下において使用する金型として、配線層の導体とは対向しない部位に配線層厚以上の高さの凸部を設け、かつこの凸部以外の表面が平坦な金型を使用して成形する請求項３記載のビルドアップ多層配線基板の製造方法。

【請求項６】ベース基板の配線層側に表面の平坦な金型を設置し、このベース基板と金型との間に溶剤を含まない流動性高分子前駆体を供給する工程（２）において、溶剤を含まない流動性前駆体を、フィルム状で供給する請求項３記載のビルドアップ多層配線基板の製造方法。

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【請求項７】ベース基板の配線層側に表面の平坦な金型を設置し、このベース基板と金型との間に溶剤を含まない流動性高分子前駆体を供給する工程（２）において、溶剤を含まない流動性前駆体を、離型処理した金型あるいはベース基板の少なくとも一方に、室温下あるいは溶融させて硬化させることなく塗布して膜状あるいはフィルム状で供給する請求項３記載のビルドアップ多層配線基板の製造方法。

【請求項８】金型とベース基板との間を排気する工程（３）、金型をベース基板方向へ移動させて溶剤を含まない流動性高分子前駆体をベース基板上の少なくとも隣接する導体間隙と貫通めっきスルーホール内に充填する工程（４）、溶剤を含まない流動性高分子前駆体に所定の静水圧をかける工程（５）により、ベース基板上の配線導体とは電気的に独立の導体金属パターンの少なくとも１部と金型を接触させて金型の移動を止める請求項３記載のビルドアップ多層配線基板の製造方法。

【請求項９】金型とベース基板との間を排気する工程（３）、金型をベース基板方向へ移動させて溶剤を含まない流動性高分子前駆体をベース基板上の少なくとも隣接する導体間隙と貫通めっきスルーホール内に充填する工程（４）、溶剤を含まない流動性高分子前駆体に所定の静水圧をかける工程（５）により、ベース基板と金型の凸部の少なくとも１部を接触させて金型の移動を止める請求項５記載のビルドアップ多層配線基板の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ビルドアップ多層配線基板及びその製造方法に係り、特に、大型計算機、ワークステーション、パーソナルコンピュータ、マルチメディアコンピュータ等のコンピュータ、通信用ＡＴＭ交換機や携帯電話、ビデオカメラ等の民生機器等に用いられる高密度な多層配線基板やマルチチップモジュール基板等に好適なビルドアップ多層配線基板及びその製造方法に関する。

【０００２】

【従来の技術】電子機器の高性能化、また、軽薄短小化に不可欠となってきているビルドアップ基板には、各種のものが提案されている。例えば特開平４－１４８５９０号公報等に開示されるように、図９に示す表裏の導通をとるためにドリル加工した貫通穴９０１があり、配線密度の向上、配線設計の自由度に制限があった。そのため、最近では、図１０に示すように、このような貫通穴を樹脂や導電性ペースト１００１などで埋めた基板上に配線領域をロスすること無くビルドアップ層１００３を積層することでこのような問題を回避する穴埋めビルドアップ基板が主流になってきている。

【０００３】穴埋めの方法としては、「合同公開研究会ビルドアップ配線板および微細印刷技術」講演要旨

集、１７～２２、３８～５１ページ（１９９７）や特開平５－６７８７４号公報等にも記載があるように、専用のインクをスクリーン印刷で穴内に充填し、紫外線や熱処理により硬化している。また、穴のサイズは、径が０．３㎜、長さ（すなわち基板厚）が０．６㎜といったところが、ビルドアップ基板の内層基板ということもあって、一般的である。

【０００４】このような従来の技術には、以下のような問題点があった。その第１の問題は、ビルドアップ層の多層化のためには、内層基板の最外配線層のために発生する各層の凸凹形状を研磨して平坦化する必要がある上に、穴埋め工程を必要とする分、従来のビルドアップ基板に比べてさらに製造工程が長くなる点である。

【０００５】第２の問題は、穴埋めインクには流動性（充填性）や光透過性が必要なため、材料が限定されることであり、したがって、硬化後のインクにも耐熱性、耐薬品性等の物性に限界が生じ、プロセス条件の厳しい高性能基板への適用の障害となっている。

【０００６】また、第３の問題は、穴埋め工程が長いことが挙げられる。これは、スクリーン印刷の性質上、充填穴周辺にインクが残り、その除去と次層の配線を形成するために基板表面を研磨して平坦にする工程が必要であるためである。さらに、第４の問題は、現実には、専用インクでも充填可能な穴のアスペクト比や、充填可能な単位面積当たりの穴数にも限界がある。

【０００７】そこで、これらの問題点を解決するために本発明者等は、特開平６－３３４３４３号公報に記載したように、金型をベース基板方向へ移動させて溶剤を含まない流動性高分子前駆体をベース基板上の少なくとも隣接する導体間隙と貫通めっきスルーホール内に充填する製造方法を提案した。

【０００８】

【発明が解決しようとする課題】このように形成された最外配線上とスルーホール内の絶縁層には、ボイドは無く、基板表面も金型面が転写されて平坦であると云う点では他の従来技術に比して格段に優れている。しかし、高密度多層基板においては、ベース基板が薄いことから基板が反り易く、これを内層基板としてビルトアップ方式で多層化を図るに際しては信頼性が低下すると云う新たな問題が発生した。また、構造的にも高密度の配線基板においては内層基板の最外配線層を電磁シールすることが重要であり、これについては格別の配慮がされていなかった。

【０００９】したがって、本発明の目的は上記従来の問題点を解消することにあり、第１の目的は内層基板の最外配線層を取り囲むように内層基板の周縁部を額縁状の導体パターンで取り巻き、同一平面上に形成された回路を電磁シールドすることによって信頼性の高いビルトアップ多層基板を実現することにあり、第２の目的は薄いベース基板を用いても信頼性を低下させずにビルトアップ方式で多層化できる改良されたビルトアップ多層基板の製造方法を実現することにある。

【００１０】

【課題を解決するための手段】上記第１の目的は、両面を電気的に接続する貫通めっきスルーホールと、少なくとも一方の面上に水平配線導体からなる配線層とを有する内層基板を備えたビルドアップ多層配線基板において、前記内層基板上の配線層とは電気的に独立で、前記配線層を取り囲むように内層基板の周縁部に形成された額縁状の導体金属パターンが配設されていることを特徴とするビルドアップ多層配線基板によって、達成される。

【００１１】そして好ましくは、額縁状の導体金属パターンを、同一面上に形成された配線層よりも厚くし、かつ少なくとも前配線層上には、前記額縁状の導体金属パターンの高さで規制され、前記額縁状の導体金属パターンと略同一平面を形成する層間絶縁層が配設された構成とすることである。

【００１２】また、上記第２の目的は、内層基板上に層間絶縁層と配線層とを交互に積層形成するビルドアップ多層配線基板の製造方法であって、前記内層基板を下記（１）～（６）の工程で順次形成することを特徴とするビルドアップ多層配線基板の製造方法によって達成される。

【００１３】（１）両面を電気的に接続する貫通めっきスルーホールと、少なくとも一方の面上に水平配線導体からなる配線層と、前記配線層とは電気的に独立で前記配線層を取り囲むように基板の周縁部に額縁状に形成された導体金属パターンとを有するベース基板を形成する工程、（２）ベース基板の配線層側に表面の平坦な金型を設置し、このベース基板と金型との間に溶剤を含まない流動性高分子前駆体を供給する工程、（３）金型とベース基板との間を排気する工程、（４）金型をベース基板方向へ移動させて溶剤を含まない流動性高分子前駆体をベース基板上の少なくとも隣接する導体間隙と貫通めっきスルーホール内に充填する工程、（５）溶剤を含まない流動性高分子前駆体に所定の静水圧をかける工程、（６）静水圧下において溶剤を含まない流動性高分子前駆体を硬化する工程及び（７）金型から内層基板を取り出す工程。

【００１４】そして、好ましくは（１）の工程においては、配線層の形成と同一工程で導体金属パターンを形成し、次いで選択的に導体金属パターン上にめっき処理し、めっき厚さ分だけかさ上げされた前記配線層厚以上の導体金属パターンを形成する工程を含み、また、（２）の工程以下において使用する金型として、配線層の導体とは対向しない部位に配線層厚以上の高さの凸部を設け、かつこの凸部以外の表面が平坦な金型を使用して成形することである。

【００１５】

【発明の実施の形態】以下、穴埋めされた貫通めっきスルーホールを持つ４層配線基板上に、表裏面２層ずつのビルドアップ層を積層した８層配線基板の構成及び製造方法の実施の形態について説明する。

【００１６】すなわち、ビルドアップ層を積層する内層基板１００及び１００´の断面構造を、図１（ａ）、図１（ｂ）に示す。絶縁材料で充填された貫通めっきスルーホール１０１と、最外配線層１０２と、最外配線層を取り囲むように基板の周縁に形成した額縁状の導体パターン１０４と、絶縁層１０３からなる配線基板とし、貫通めっきスルーホール内に充填される絶縁材料と基板の最外絶縁層１０３とを同一材料で形成し、かつ、基板表面が平坦な構造とした。

【００１７】絶縁材料で充填された貫通めっきスルーホール１０１の直径は１～１０００μｍの範囲から、また、長さ（すなわち内層基板厚）は０．０５～５ｍｍの範囲から任意に選択可能であり、基板表面の平坦性は、図１（ａ）の構造の場合、額縁状の導体パターン１０４及び最外配線層１０２の導体間隙を埋めた最外絶縁層１０３の厚さとこれら導体層の厚さとの差が導体層の厚さの１０％以内、あるいは、図１（ｂ）の構造の場合、額縁状の導体パターン１０４及び最外配線層１０２の導体間隙を埋め、かつ、これら導体層を覆う絶縁層１０３の厚さバラツキが絶縁層厚の１０％以内である。

【００１８】ビルドアップ多層基板を製造するには、図１の内層基板上に周知の積層化技術によって配線層と絶縁層とを交互に形成すればよい。図１（ｂ）に示すように、額縁状の導体パターン１０４及び最外配線層１０２上を最外絶縁層１０３で覆われた構造の場合には、次層のビルドアップ層との電気的接続は、図２に示すような最外絶縁膜１０３に導体１０２が露出するまでレーザ加工した穴内１０５に、めっき法により図３に示すような従来のビルドアップ基板方式３０１や図４のような無電解めっき４０１による充填めっきで５層目及び６層目の配線導体パターンを形成して行えば良い。このような穴１０５の直径は、ビルドアップ基板用感光性層間絶縁膜材料では形成不可能な１～５０μｍで加工が可能で、絶縁層表面の穴径が導体の露出径以上（テーパ形状）であることが望ましい。

【００１９】また、レーザ加工によって絶縁膜に穴を明ける際のレーザ種としては、低コストなＹＡＧ、あるいは、炭酸レーザが好ましい。上記レーザ加工した穴内１０５に配線を形成する前に、穴内壁および底部を含む基板表面５０３を酸化性液体処理やドライ洗浄処理により、清浄、粗面化及び親水化しておけば、形成する配線の接続信頼性が向上するだけでなく、図３のような穴内の配線と内層基板表面の配線との同時形成の歩留りが向上する。

【００２０】このような酸化性液体としては、アルカリ性過マンガン酸カリウム水溶液、あるいは、濃硫酸とクロム酸の混酸が好ましいが、環境面からより好ましいのはアルカリ性過マンガン酸カリウム水溶液である。また、ドライ洗浄処理としては、酸素プラズマアッシング、ＵＶ／オゾン処理、あるいは、コロナ放電のうちの少なくとも１つの方法であることが望ましい。

【００２１】さらに、このレーザ穴のアスペクト比が大きくなると、例えば特開平８－７８８４６号公報に開示されるように、図５に示すように、穴内を完全に充填した上に充填部５０１を平坦に、内層基板表面配線部５０２と同一面にすることができる。

【００２２】図５に示した表面配線部５０２は、５層目及び６層目の配線導体パターンとなるが、この後は、周知の絶縁層と導体層との形成工程を繰り返すことにより７層目及び８層目のパターンを積層することができる。

【００２３】次に、図１で示したビルドアップ基板用内層基板の形成工程について、図６の工程図を用いて説明する。ただし、内層基板１００を形成するためのベース基板６０３は４層配線を形成しているが、ここでは内層部を省略し最外層部のみを表示してある。

【００２４】（１）先ず、図６（ａ）に示すように、両面を電気的に接続する貫通めっきスルーホール６０１を有し、少なくとも一方の面上に水平配線導体からなる配線層１０２と、この配線層とは電気的に独立で配線層を取り囲むように基板の周縁部に額縁状に形成された導体金属パターン１０４とを有するベース基板６０３を形成する。なお、導体金属パターン１０４は、配線層１０２と同一のパターン形成工程で形成するが、配線層１０２とは別工程により、異なる材質の導体で形成してもよい。

【００２５】（２）図６（ｂ）に示すように、ベース基板６０３の配線層側に表面の平坦な金型６０４を設置し、このベース基板と金型との間に溶剤を含まない流動性高分子前駆体（絶縁層を形成する原料樹脂）６０５を供給する。なお、６０７は金型の上下を封止する弾性体からなるパッキンで、ここではシリコーンゴム製のパッキンを使用している。

【００２６】（３）図６（ｂ）→図６（ｃ）に示すように、金型６０４とベース基板６０３との間を排気口６０６より排気する。

【００２７】（４）図６（ｃ）→（ｄ）に示すように、金型をベース基板方向へ移動させて溶剤を含まない流動性高分子前駆体６０５をベース基板上の少なくとも隣接する導体間隙と貫通めっきスルーホール内に充填する。充填を容易にするため金型を所定温度に昇温し高分子前駆体６０５の流動性を高める。金型の移動量は、配線層１０２及び基板の周縁部に額縁状に形成された導体金属パターン１０４の表面に金型の平面が接触するまでとする。

【００２８】（５）図６（ｄ）に示すように、溶剤を含まない流動性高分子前駆体６０５に、付加口６０６より

窒素、空気等の不活性ガスを注入して所定の静水圧をかける。

【００２９】（６）図６（ｄ）→（ｅ）に示すように、静水圧下において溶剤を含まない流動性高分子前駆体を硬化し、型抜きをする。

【００３０】以上の工程により、配線層１０２及び基板周縁部に額縁状に形成された導体金属パターン１０４の表面を露出しつつ、隣合う配線層１０２間及び配線層１０２と導体パターン１０４との間隙を絶縁層１０２で充填すると共に、同時にスルーホール６０１内も絶縁層１０２で充填されたスルーホール１０１を有する内層基板１００が得られる。

【００３１】また、上記工程（１）の変形例として、図７（ａ）に示したよに、基板周縁部に額縁状に形成した導体パターン１０４（配線層１０２とは電気的に独立）の上に、導体めっきして配線層厚以上の高さの導体金属パターン７０２を形成しておく。この導体金属パターン７０２の高さで、その後に配線層１０２上に積層される絶縁層１０３の厚さを規制する。

【００３２】上記の工程（３）、（４）、（５）の後、この導体金属パターン７０２の少なくとも１部と金型の平面とを接触させて金型の移動を止め、静水圧下において溶剤を含まない流動性高分子前駆体を硬化すれば、図７（ｂ）に示したように、ベース基板７０３の最外配線層１０２上にビルドアップ絶縁層７０５を形成すると共に、同時に、貫通めっきスルーホール６０１の穴埋め７０６もできる。

【００３３】導体金属パターン７０２の形成位置に制限はないが、絶縁層厚を高精度に制御するためには、少なくとも、ベース基板外周部の導体パターン１０４上には必要であり、望ましくは、配線領域外周部にも設けるべきである。

【００３４】このように形成された最外配線層上とスルーホール内の絶縁層には、本発明者等が先に提案した特開平６－３３４３４３号公報に開示するように、ボイドは無く、表面も金型面が転写されて平坦である。さらに、本製造方法では、加熱下で（４）以降の工程の実施が可能で、室温で流動性の無い固形の溶剤を含まない流動性高分子前駆体でも加熱溶融して低粘度化させて使用が可能になり、材料選択の幅が広がる。したがって、粘度上昇を引き起こすことになっても材料中のフィラ含有量を調整し、熱膨張係数をベース基板に合わせて穴埋め部の凹み、膨らみを抑制することができる。

【００３５】さらに、スルーホール内を排気した後、穴埋めするので厚いベース基板や薄板ながら小径でアスペクト比の高い貫通めっきスルーホールを持つベース基板の適用も可能である。また、実際には、導体金属パターン７０２にほぼ接するまで金型は移動するので、これらの間に残る絶縁膜は数μｍ程度で、その量も導体金属パターン７０２の形成精度に依存して、やや低い導体金属パターン部に膜が残るだけである。したがって、最外絶縁膜厚７０５は、導体金属パターン７０２の厚さで制御でき、このような導体金属パターンの形成方法としては、めっき法が一般的で、より高い精度が必要な場合は、無電解めっき方が好ましく、むしろ形成時間を重視するならば電気めっき法が良い。図７に示すように、このようなめっきを行う下地となる額縁状の導体パターン１０４を、配線層を形成する際に同時に形成しておくので、めっき量が短縮されて、導体金属パターンの形成精度を向上させ、形成時間を短縮できる。

【００３６】上記のように最外配線層上に絶縁層を形成する場合、配線導体とは電気的に独立な配線層厚以上の高さの導体金属パターン７０２の変わりに、逆に、図８に示すように、絶縁層厚制御用の凸部８０１を金型６０６に設けてもかまわない。このような凸部も配線層の導体と対向しない部位で、少なくとも、ベース基板外周部には必要であり、配線領域外周部にもあることが望ましい。その形成は、金型表面を適当な機械加工法で切削しても良いし、めっきあるいはそれに続くエッチングで行っても構わない。また、正確な寸法の凸形状用の部材を金型に接着、溶接等したものも使用できる。

【００３７】本発明においては内層基板の絶縁層を構成する樹脂として、溶剤を含まない流動性高分子前駆体を用いるが、これは金型を用いて樹脂を配線層間やスルーホールに充填する際にガスの発生を抑制したいからである。溶剤を含むと充填時にガスが発生して絶縁層内にボイドが発生し、絶縁特性を著しく劣化させるからである。溶剤を含まない流動性高分子前駆体は、熱膨張係数調整用や粗化面態形成用のフィラを含有する熱硬化性樹脂や熱可塑性樹脂であり、液状のものも固形のものもある。これらは、液状の場合は、離型処理した金型あるいはベース基板の少なくとも一方に塗布した液膜状として使用すれば良いし、固形の場合は、フィルム状や、離型処理した金型あるいはベース基板の少なくとも一方に溶融させて硬化させることなく固着したフィルム状として使用できる。

【００３８】

【実施例】以下、本発明を、穴埋めされた貫通めっきスルーホールを持つ４層配線基板上に、表裏面２層ずつのビルドアップ層を積層した８層配線基板の構成と製造方法とを実施例により具体的に説明する。

【００３９】〈実施例１〉

図１１に示す構造の８層配線基板の製造方法を以下に示す。製造工程は、図６に示した工程図にしたがう。先ず、図１１の中央部の層に該当するベース基板（図６（ａ）の６０３に該当）を製造する。ガラスエポキシ基板（ガラス繊維にエポキシ樹脂を含浸した積層板）の両面に銅箔を張り合わせた５００ｍｍ角、板厚１．６ｍｍの両面銅張積層板の３５μｍ厚銅箔をエッチングして第４配線層１１０４と第５配線層１１０５を形成した基板

の両面に、０．１mm厚のプリプレグ（ガラスエポキシ基板）を２枚づつ挟んで１８μm厚銅箔を重ね、積層接着した。

【００４０】作製した両面板に０．２mm直径のドリルで３５０００個の貫通穴明け加工をした後、パネルめっきをし、両面の銅箔をエッチングして配線パターンを形成してから、貫通めっきスルーホール１１０９、第３配線層１１０３、第６配線層１１０６及び基板周縁部に額縁状に形成した導体パターン１０４（配線層１１０３、１１０６とは電気的に独立）を形成したベース基板を作製した。これは図６（ａ）工程に該当する。

【００４１】以下の工程は、図６（ｂ）～図６（ｅ）で説明した手順にしたがって行う。平均粒径２μmのシリカフィラを５０体積％混合したビフェニル系エポキシ樹脂とフェノール樹脂の組成物を８０℃で溶融させ、フッ素系耐熱離型剤を塗布した表面が平坦な平板状の金型上に流し、空冷してフィルム状に溶融固着した。

【００４２】この金型２枚の間に先に作製したベース基板を挟み、金型間を１０Ｔｏｒｒに排気し、金型を７０℃に加熱してエポキシ組成物を溶融させ、第３、第６配線間、貫通めっきスルーホール内に充填した。そして、排気を止め、金型を挟み付ける圧縮圧力０．９ＭＰａと金型間に空気圧０．８ＭＰａを付加し、金型を第３、第６配線層まで移動させ、静水圧下、金型を加熱して１６０℃で３０分間、１８０℃で６０分間、エポキシ組成物を硬化し、最外配線層導体間と貫通めっきスルーホールが無欠陥な同一絶縁材料で充填された平坦なビルドアップ基板用４層配線の内層基板１１１０を作製した。

【００４３】次いで、上記内層基板１１１０を過マンガン酸カリウム－水酸化ナトリウム水溶液中、８０℃で４５分間、３％硫酸ヒドロキシルアミン水溶液中、２３℃で５分間処理して第３、第６配線層導体上を清浄化し、層間絶縁層として市販の感光性層間絶縁材料を使用して周知の積層パターンの形成方法により、第１配線層１１０１、第２配線層１１０２を含むビルドアップ層１１１１を積層して、研磨すること無く配線総数８層のビルドアップ積層基板を製造した。

【００４４】このビルドアップ積層基板は、内層基板１１１０の周縁部に額縁状の導体パターン１０４が形成されていることから、ビルドアップ層１１１１を積層する際に、そりが発生することなく、しかも額縁状の導体パターン１０４がその内部領域の配線層を電磁シールドする効果を有するため信頼性の高い高密度多層配線基板が実現できた。また、基板周縁部に形成された額縁状の導体パターン１０４は、金型で内層基板を静水圧下で製造する際に、パッキンの作用効果をも有している。

【００４５】〈実施例２〉

図１２に示す構造の８層配線基板の製造方法を以下に示す。実施例１と同様にベース基板を作製する際に、第３配線層１２０３と第６配線層１２０６の形成時に、基板外周を１０mm幅で取り囲むようにこれら配線層とは電気的に独立した額縁パターン１２０９を残し、さらに、この部分にのみ電気めっきにより５０±２μm厚のめっき銅１２１０を形成しておく。そして、実施例１と同様にしてエポキシ系絶縁層を形成して、最外配線層上及び導体間と貫通めっきスルーホールが無欠陥な同一絶縁材料で被覆及び充填された、平坦なビルドアップ絶縁層１２１１（５２±１μm厚）をすでに１層形成したビルドアップ基板用４層配線の内層基板１２１２を作製した。

【００４６】次いで、炭酸ガスレーザ装置により第３、第６配線層上のビルドアップ絶縁層１２１１の所定の位置に上径５０μm、底径４０μmの円筒状穴を明け、この内層基板を過マンガン酸カリウム－水酸化ナトリウム水溶液中、８０℃で４０分間、３％硫酸ヒドロキシルアミン水溶液中、２３℃で５分間処理してから両面に１μm厚の無電解めっき銅膜を形成した。レーザ穴部を含む所定の位置に穴明け加工をしたドライフィルムレジストを成膜し、電気めっきにより第２配線層１２０２、第７配線層１２０７の導体パターンを形成してドライフィルムを剥離、無電解めっき銅膜の配線以外の部分をエッチング除去した。さらに、市販のレーザ加工用層間絶縁材料を使用して１層積層し、ビルドアップ層１２１３を形成し、配線総数８層のビルドアップ基板を製造した。

【００４７】内層基板１２１２の最外配線層と同一工程で形成した基板周縁部の配額縁パターン１２０９は、実施例１と同様の効果を有しているが、本実施例においてはさらにその上に形成しためっき銅パターン１２１０の厚さを制御することにより、平坦なビルドアップ絶縁層１２１１の膜厚を正確に規制できるという効果を有している。

【００４８】〈実施例３〉

図１３に示す構造の８層配線基板の製造方法を以下に示す。実施例１と同様にベース基板を作製した。ベース基板の外周部、第３配線層１３０３や第６配線層１３０６を１０mm幅で額縁状に取り囲む位置１３０９に対向する部分が１００μmの高さに残るように研削研磨して作製した表面が平坦なステンレス製の金型を使用し、実施例２と同様に、最外配線層上及び導体間と貫通めっきスルーホールが無欠陥な同一絶縁材料で被覆及び充填された、平坦なビルドアップ絶縁層１３１０をすでに１層形成したビルドアップ基板用４層配線の内層基板１３１１を作製した。

【００４９】さらに実施例２と同様にして、ＹＡＧレーザ装置により第３、第６配線層上のビルドアップ絶縁層１３１０の所定の位置に上径３０μm、底径２５μmの円筒状穴を明け、この内層基板を過マンガン酸カリウム－水酸化ナトリウム水溶液／３％硫酸ヒドロキシルアミン水溶液で処理し、さらに酸素プラズマアッシャ処理をして両面に１μm厚の無電解めっき銅膜を形成した。レーザ穴部を含む所定の位置に穴明け加工をしたドライフ

ィルムレジストを成膜し、電気めっきにより、レーザ穴内１３１２が完全に充填されたうえに平坦な第２配線層１３０２、第７配線層１３０７の導体パターンを形成してドライフィルムを剥離、無電解めっき銅膜の配線以外の部分をエッチング除去した。さらに、市販のレーザ加工用層間絶縁材料を使用して１層積層し、ビルドアップ層１３１３を形成し、配線総数８層のビルドアップ基板を製造した。

【００５０】内層基板１３１１の周縁部に設けた額縁状の導体パターン１０４の効果は、実施例１の場合と同様に得られた。本実施例ではさらにビルドアップ絶縁層１３１０の外周が内側に寄ってベース基板の外周部１３０９を露出しているため、導体パターン１０４及びビルドアップ絶縁層１３１０の外周部を保護することができ信頼性をさらに高めている。

【００５１】〈実施例４〉

実施例１において、絶縁層を形成するエポキシ組成物を、平均粒径１．５μmのシリカフィラを５０体積％混合したビスフェノールＡ系エポキシ樹脂とジシアンジアミドの組成物に代え、これをベース基板上面と下面に対向する金型上に室温で塗布して供給した。そして、金型間を室温で５分間排気した後は同様に操作して、図１１に示す構造のビルドアップ基板を製造した。

【００５２】〈実施例５〉

実施例２において、絶縁層を形成するエポキシ組成物を、平均粒径１．５μmのシリカフィラを５０体積％混合したビスフェノールＡ系エポキシ樹脂とジシアンジアミドの組成物に代え、これをベース基板上面と下面に対向する金型上に室温で塗布して供給した。ベース基板は板厚４．０mmのものを使用し、実施例４同様に操作して、図１２に示す構造のビルドアップ基板を製造した。なお、過マンガン酸カリウム－水酸化ナトリウム処理時間は３０分にした。

【００５３】〈実施例６〉

実施例３において、絶縁層を形成するエポキシ組成物を、平均粒径１．５μmのシリカフィラを５０体積％混合したビスフェノールＡ系エポキシ樹脂とジシアンジアミドの組成物に代え、これをベース基板上面と下面に対向する金型上に室温で塗布して供給した。ベース基板は板厚０．３mmで、炭酸ガスレーザにより作製した仕上がり径３０μmの貫通めっきスルーホールを設けたものを使用し、実施例４同様に操作して、図１３に示す構造のビルドアップ基板を製造した。なお、過マンガン酸カリウム－水酸化ナトリウム処理時間は３０分にした。

【００５４】〈実施例７〉

実施例５において、絶縁層を形成するエポキシ組成物を、平均粒径１．５μmのシリカフィラを４０体積％混合した液状ＢＴレジン（ビスマレイミドートリアジンレジン：三菱ガス化学製）に代え、図１２に示す構造のビルドアップ基板を製造した。硬化条件は１６０℃３０分、２２０℃６０分、過マンガン酸カリウム－水酸化ナトリウム処理時間は２０分にした。

【００５５】

【発明の効果】上述したように、本発明により所期の目的を達成することができた。すなわち、内層基板の最外配線層を取り囲むように内層基板の周縁部を額縁状の導体パターンで取り巻き、同一平面上に形成された回路を電磁シールドすることによって信頼性の高いビルトアップ多層基板を実現することができた。

【００５６】また、薄い内層基板を用いても信頼性を低下させずにビルトアップ方式で多層化できる改良されたビルトアップ多層基板の製造方法を実現することができた。

【００５７】具体的には、ビルドアップ層を積層するための内層基板を、絶縁材料で充填された貫通めっきスルーホールと、同一絶縁材料で少なくとも最外配線層間及び最外配線層と基板周縁に設けた額縁状の導体パターンとの間隙を埋め込んだ絶縁層とで構成し、かつ基板表面を平坦な構造とすることにより、額縁状の導体パターンが基板の反りを防止し、同一平面内に形成された配線層を磁気シールドする効果を有し、ビルドアップ多層基板の信頼性と歩留まりを格段に向上させることができた。

【００５８】内層基板の最外層の配線層とは電気的に独立に内層基板の周縁部に額縁状の導体パターンを形成した後、さらにこの導体パターン上に配線層厚以上の高さの第２の導体金属パターンを設けておけば、最外配線層上に、これら導体金属パターン類で膜厚制御された平坦な絶縁層を形成すると同時に貫通めっきスルーホールの穴埋めができる。

【００５９】また、本工程は加熱下でも実施可能なため、流動性に劣る高粘度な穴埋め材料でも必要に応じて溶融させて粘度を下げた状態で使用することができる。したがって、熱膨張係数を下げるために、粘度は上がるにもかかわらず、フィラ含量を増やし、材料構成を最適化して対応することが可能となり、内層基板の表面を研磨等特別な工程無しに平坦に形成することができるし、また、同時にビルドアップ層を積層するためにプロセス上必要な耐熱性、耐薬品性も付与することができる。さらに本工程では、一旦、貫通めっきスルーホール内を排気した後、穴埋め材料を流動させて充填するので、本質的に充填の欠陥は無く、単位面積当たりの穴数の影響も受けない。

【図面の簡単な説明】

【図１】本発明に係るビルドアップ基板用内層基板の構造の一例を示す断面図。

【図２】本発明に係るビルドアップ基板用内層基板の構造の一例を示す断面図。

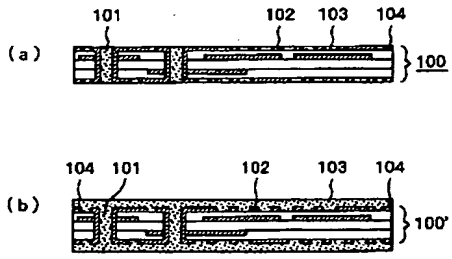
【図３】本発明に係るビルドアップ基板用内層基板とビルドアップ層との電気的接続形態の一例を示す断面図。

【図４】本発明に係るビルドアップ基板用内層基板とビ

ルドアップ層との電気的接続形態の一例を示す断面図。
【図５】本発明に係るビルドアップ基板用内層基板とビルドアップ層との電気的接続形態の一例を示す断面図。
【図６】本発明に係るビルドアップ基板用内層基板の製造方法の一例を示す工程図。
【図７】本発明に係るビルドアップ基板用内層基板の製造方法の一例を示す工程図。
【図８】本発明に係るビルドアップ基板用内層基板の製造方法の一例を示す工程図。
【図９】従来のビルドアップ基板の構造の一例を示す断面図。
【図１０】従来のビルドアップ基板の構造の一例を示す断面図。
【図１１】本発明に係るビルドアップ基板の構造の一例を示す断面図。
【図１２】本発明に係るビルドアップ基板の構造の一例を示す断面図。
【図１３】本発明に係るビルドアップ基板の構造の一例を示す断面図。
【符号の説明】
１００、１００′…内層基板、
１０１…貫通めっきスルーホール、
１０２…配線層、
１０３…絶縁層、
１０４…額縁状導体パターン、
１０５…レーザ加工穴内部、
３０１…従来のビルドアップ基板方式で形成した上層接続用の配線導体、
４０１…無電解めっきで形成した上層接続用の配線導体、
５０１…配線導体で充填したレーザ穴上部、
５０２…内層基板表面配線層、
５０３…内層基板表面、
６０１…貫通めっきスルーホール、
６０３…ベース基板、
６０４…金型、
６０５…溶剤を含まない流動性高分子前駆体、
６０６…排気口、静水圧付加口、
６０７…パッキン、
７０２…導体金属パターン、
７０５…ビルドアップ絶縁層、
７０６…貫通めっきスルーホールの穴埋め部、
８０１…絶縁層厚制御用の凸部、
９０１…貫通めっきスルーホール、
９０２…ビルドアップ基板用内層基板、
９０３…ビルドアップ層、
１００１…穴埋め樹脂、導電性ペースト、
１００２…ビルドアップ基板用内層基板、
１００３…ビルドアップ層、
１１０１、１２０１、１３０１…第１配線層、
１１０２、１２０２、１３０２…第２配線層、
１１０３、１２０３、１３０３…第３配線層、
１１０４、１２０４、１３０４…第４配線層、
１１０５、１２０５、１３０５…第５配線層、
１１０６、１２０６、１３０６…第６配線層、
１２０７、１３０７…第７配線層、
１２０８、１３０８…第８配線層
１１０９…貫通めっきスルーホール、
１１１０…ビルドアップ基板用内層基板、
１１１１…ビルドアップ層、
１２０９…額縁パターン、
１２１０…めっき銅、
１２１１…ビルドアップ絶縁層、
１２１２…ビルドアップ基板用内層基板、
１２１３…ビルドアップ層、
１３０９…ベース基板外周部、
１３１０…ビルドアップ絶縁層、
１３１１…ビルドアップ基板用内層基板、
１３１２…レーザ穴内部、
１３１３…ビルドアップ層。

【図１】

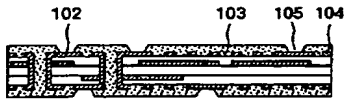
図 1



１００、１００′…内層基板　１０１…貫通めっきスルーホール
１０２…配線層　１０３…絶縁層　１０４…額縁状導体パターン

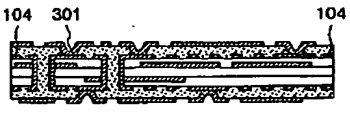
【図２】

図 2



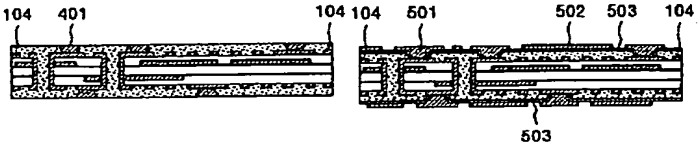
【図３】

図 3



【図４】

図 4

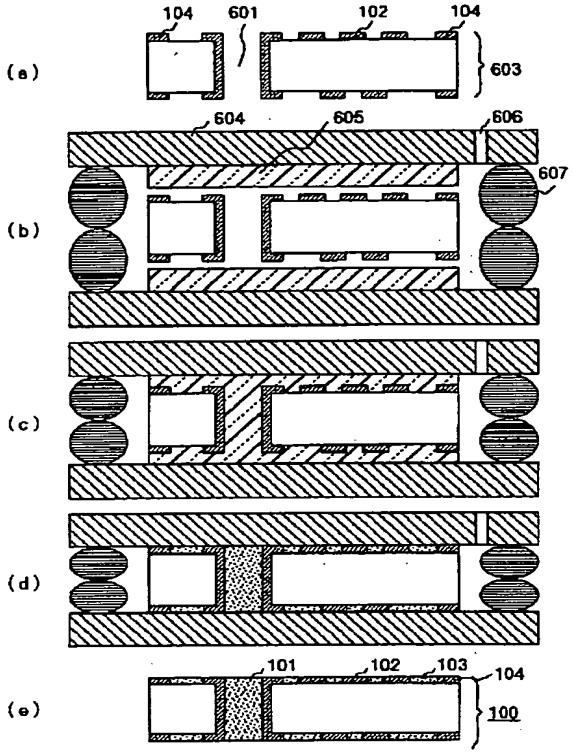


【図５】

図 5

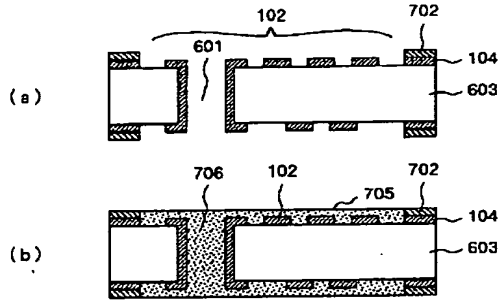
【図６】

図 6



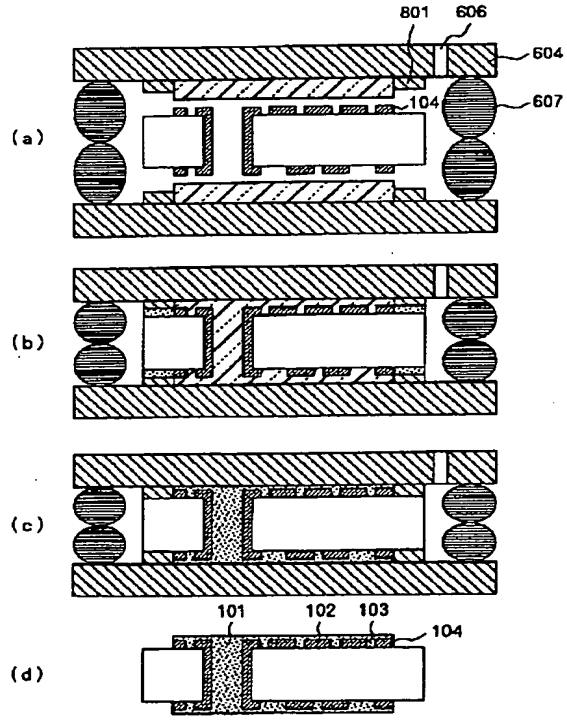
【図７】

図 7



【図８】

図 8

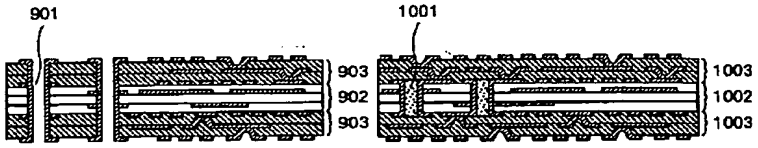


【図９】

図 9

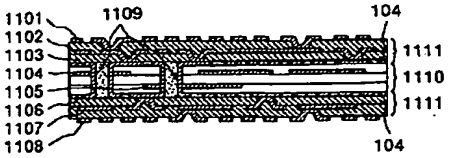
【図１０】

図 10



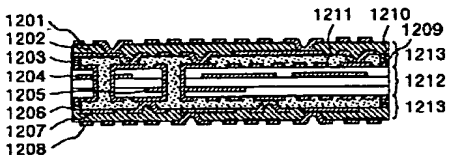
【図１１】

図 11



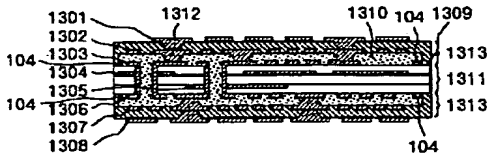
【図１２】

図　１２



【図１３】

図　１３



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